

Towards generation of 1D device structures beyond expected scaling limits

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The relentless miniaturisation of electronic circuitry has spawned the ICT revolution that has impacted every aspect of modern life. However, this trend in scaling is facing a number of significant challenges if the progress defined in International roadmaps is to be delivered. As well as facing significant barriers associated with fundamental limits such as interconnect related delay times and power issues there is the cost of improving light sources for photolithography and implementing new mask/resist technologies.

A vision for the industry is to implement bottom-up substrate patterning methods using self-organisation of components rather than conventional top-down lithographies. However, this is a real challenge as the reproducibility, placement accuracy and defect densities within the pattern have very exacting requirements. Further, multi-layers of self-organised materials are required. In this presentation I will discuss recent progress in Cork in this area using self-organisation in polymer systems and inorganic systems to achieve highly regular nanopatterns. These are based around phase separation in block co-polymer systems and the use of graphoepitaxy to orientate the patterns. I will further outline methods to transfer these 'soft' patterns to the substrate in order to achieve active device-like structures. Finally, I will discuss the challenges facing the research community before these technologies could be used to fabricate mass-produced integrated device structures.